Strained Silicon-Germanium / Silicon Heterostructure Tunnel FETs for Low Power Applications

Sebastian Blaeser
Strained Silicon-Germanium/Silicon Heterostructure Tunnel FETs for Low Power Applications

Sebastian Blaeser
# Contents

Abstract i

Kurzfassung iii

1 Introduction 1

2 Theoretical Background 5
   2.1 Power Consumption in Integrated Circuits 5
   2.2 Physics of a MOSFET 6
      2.2.1 Subthreshold Characteristics 7
   2.3 Physics of a TFET 9
      2.3.1 Kane's BTBT Model 10
      2.3.2 Phonon Assisted BTBT 13
      2.3.3 Trap Assisted Tunneling 14
      2.3.4 Shockley-Read-Hall Recombination 16
      2.3.5 BTBT Mechanisms 16
   2.4 Design Considerations 19
      2.4.1 Strain Engineering 19
      2.4.2 EOT Scaling 20

3 Vertical SiGe/Si Heterostructure TFETs 25
   3.1 Device Fabrication 25
   3.2 Device Characterization and Simulation 29
      3.2.1 Design Considerations 30
      3.2.2 DC Characteristics 32
   3.3 Summary and Discussion 39

4 Planar SiGe/Si Heterostructure TFETs 41
   4.1 Device Fabrication 41
   4.2 Device Characterization and Simulation 45
      4.2.1 DC Characteristics 46
      4.2.2 Pulsed Measurements 64
      4.2.3 Low Temperature Analysis 67
      4.2.4 Logic Applications 77
   4.3 Summary and Discussion 81

5 Summary and Outlook 85
   5.1 Design Optimizations 87
Contents

Bibliography  i
List of Publications  xv
Curriculum Vitae
Acknowledgments
Strained Silicon-Germanium / Silicon Heterostructure Tunnel FETs for Low Power Applications

Sebastian Blaeser